

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

| | | |
|---------------------------------|---|--------------------------------|
| Applicant(s): Lu et al. |) | Express Mail No. EV322440308US |
| |) | |
| Serial No.: TBD |) | |
| |) | |
| Filed: herewith |) | |
| |) | |
| For: METHOD OF GENERATING AN |) | |
| EFFICIENT STUCK-AT FAULT AND |) | |
| TRANSITION DELAY FAULT |) | |
| TRUNCATED SCAN TEST PATTERN FOR |) | |
| AN INTEGRATED CIRCUIT DESIGN |) | |
| |) | |
| Group Art Unit: TBD |) | |
| |) | |
| Examiner: TBD | | |

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with 37 C.F.R. § 1.56, the references listed on the attached Form PTO-1449 are being brought to the attention of the Examiner for consideration in connection with the examination of the above-identified patent application. The Form PTO-1449 includes one (1) reference in total, listed as item AA.

This Information Disclosure Statement (IDS) is filed herewith the above-identified application, within three months of the filing date of the application, and before the mailing date of a first Office Action on the merits, and therefore, the IDS is properly submitted pursuant to 37 C.F.R. § 1.97(b), and therefore it is believed that no fee is due for the filing of this IDS. However, if a fee is required, the Commissioner is authorized to charge the unpaid amount to Deposit Account No.12-2252.

In accordance with the duty of disclosure imposed by 37 C.F.R. § 1.56 to inform the Patent Office of all references known by Applicants or Applicants' representative that may be material to the examination of the subject application, Applicants' representative hereby

provides this Information Disclosure Statement prepared in accordance with 37 C.F.R. §§ 1.97-1.98 and includes Form PTO-1449.

Copies of the items listed on Form PTO-1449 are provided pursuant to C.F.R. § 1.98(a)(2).

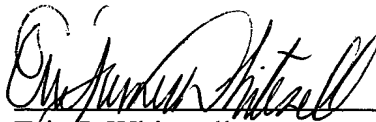
The items listed on the attached Form PTO-1449 are in the English language. Therefore, no further explanation of the listed items is required. See 37 CFR 1.98(a)(3)(ii).

Applicants respectfully request that the Examiner review the listed references and that they be made of record in the file history of the above-captioned application.

Although these documents are being made known to the Patent and Trademark Office in compliance with Applicant's duty of disclosure, such disclosure is not to be construed as an admission by Applicants or Applicants' representative that the reference is material to patentability or effective as prior art against the subject application.

The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 during its entire pendency, or credit any overpayment, to Deposit Account No. 12-2252. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 12-2252.

Dated: December 3, 2003


Eric J. Whitesell
Registration No. 38,657

ADDRESS ALL CORRESPONDENCE TO:

LSI Logic Corporation
1551 McCarthy Blvd., MS D-106
Milpitas, CA 95035
Telephone: (408) 433-8708
Facsimile: (408) 433-7770

